IN THE CLAIMS

Claims 1-17 (Canceled)

18. (Previously Presented) A semiconductor device including a MISFET, comprising:

a semiconductor substrate having a first conduction type;

a first semiconductor region having the first conduction type, formed in the semiconductor substrate;

a second semiconductor region having a second conduction type which is opposite to the first conduction type, formed over the first semiconductor region;

a third semiconductor region having the first conduction type, formed over the second semiconductor region;

an insulating film formed over the third semiconductor region;

a first hole reaching the second semiconductor region, formed in the third semiconductor region;

a second hole connected to the first hole, formed in the insulating film; and

a conductive film formed in the first and the second holes,

wherein the conductive film is electrically connected to the second and the third semiconductor regions, and

a width of the second hole is larger than a width of the first hole.

19. (Previously Presented) The semiconductor device according to claim 18, wherein:

the conductive layer in the second hole and the third semiconductor region are contacted at an upper surface and a side surface of the third semiconductor region.

20. (Previously Presented) The semiconductor device according to claim 18, wherein:

the semiconductor substrate has a main surface and a back surface,

a trench reaching the first semiconductor region is formed in the main surface of the semiconductor substrate,

a gate insulating film of the MISFET is formed in the trench, and

a gate electrode of the MISFET is formed over the gate insulating film.

21. (Previously Presented) The semiconductor device according to claim 20, wherein:

the first, the second, and the third semiconductor regions comprise a drain region, a channel-forming region, and a source region of the MISFET, respectively.

22. (Previously Presented) The semiconductor device according to claim 21, wherein:

the conductive layer in the second hole and the source region are contacted at an upper surface and a side surface of the source region.

23. (New) A method of manufacturing a semiconductor device including a MISFET, comprising the steps of:

(a) forming a trench in a semiconductor substrate;

(b) forming a gate insulating film of said MISFET on a side surface of said trench;

(c) after said step (b), selectively forming a conductive film within said trench and over an isolation region of said substrate; and

(d) forming a diode element over said isolation region,

wherein said conductive film formed in said trench serves as a gate electrode of said MISFET.